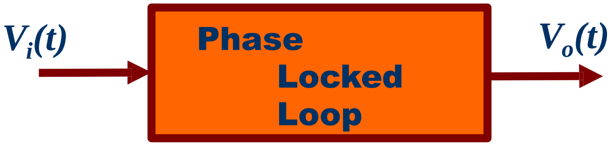
Introduction to Phase Locked Loop (PLL)

Presentation Outline

- What is Phase Locked Loop (PLL)
- Basic PLL System
- Problem of Lock Acquisition
- Phase/Frequency Detector (PFD)
- Charge Pump PLL
- Application of PLL

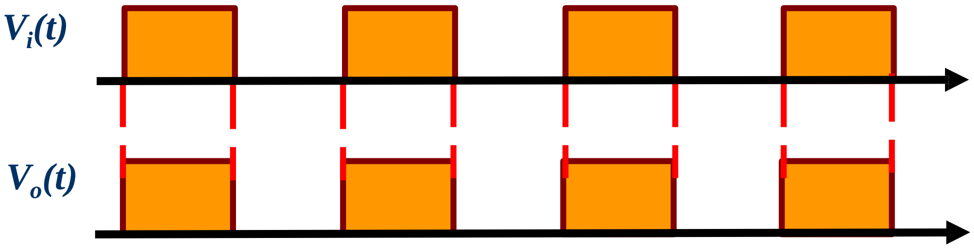
What is Phase Locked Loop (PLL)

- PLL is an ***Electronic Module*** (Circuit) that locks the ***phase*** of the output to the input.

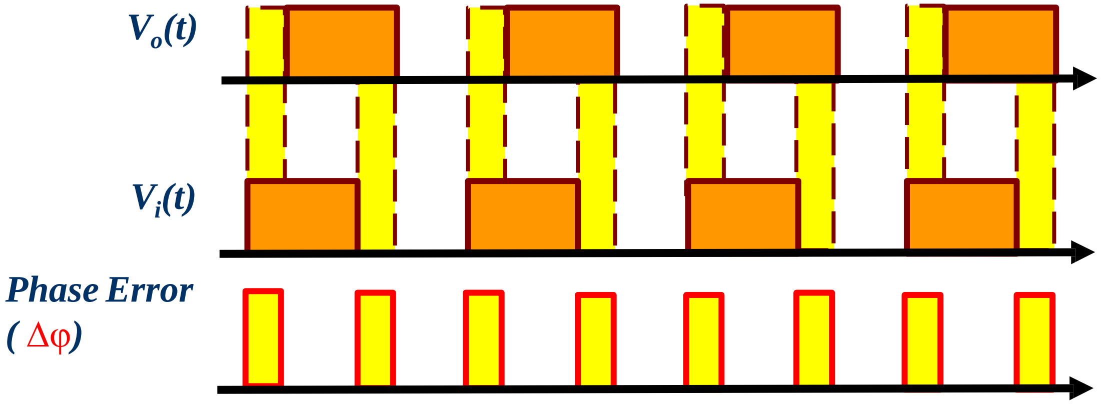


Locked Vs. Unlocked Phase

- Example of locked phase

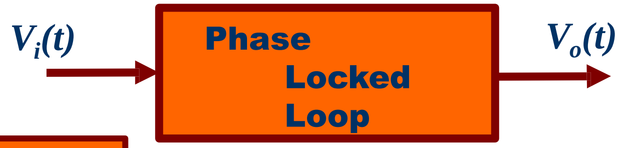


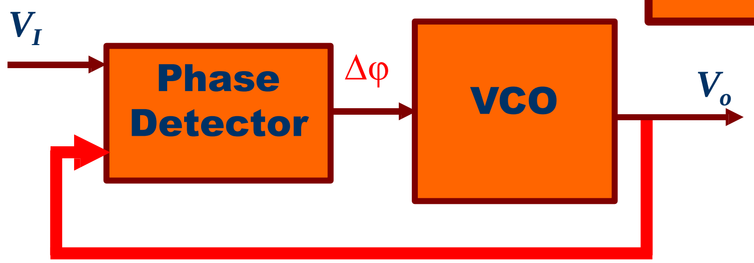
- Example of unlocked phase



Basic PLL System

- PLL is a ***feedback*** system that ***detects*** the ***phase error*** $\Delta\varphi$ and then ***adjusts*** the phase of the output.

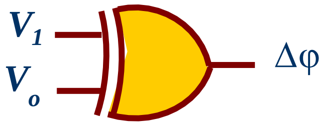


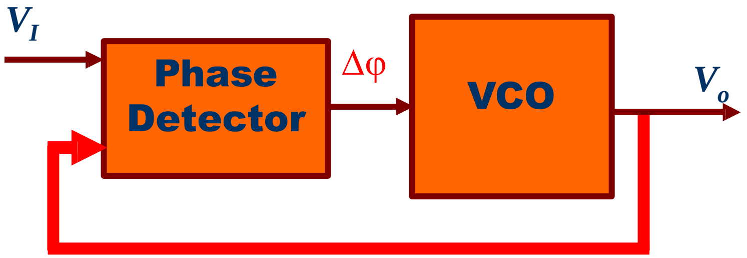


- The Phase Detector (PD), detects $\Delta\varphi$ between the output and the input through feedback system
- Voltage Control Oscillator (VCO) adjusts the phase difference

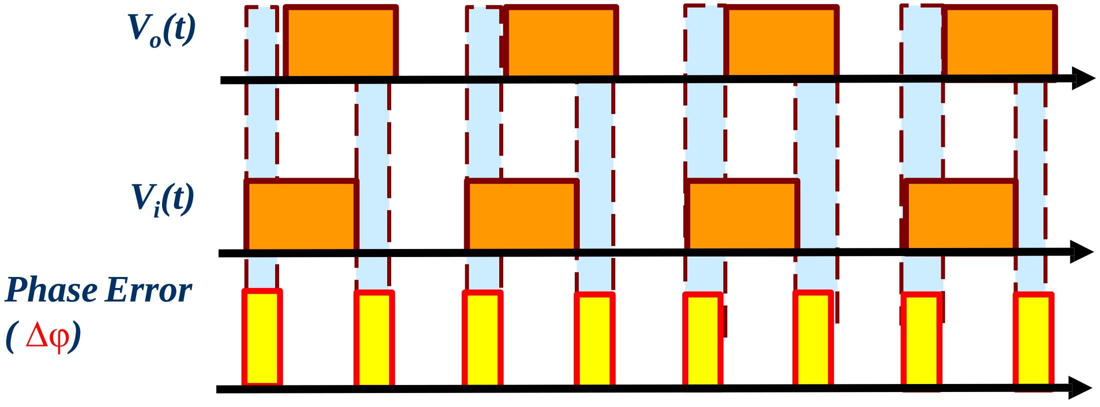
Implementation of PD

Phase Detector is an XOR gate



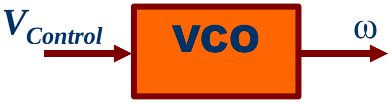


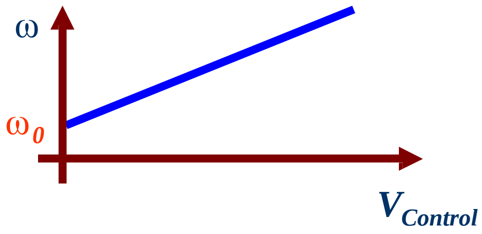
$$\Delta\varphi = \begin{cases} 1 & V_I \neq V_o \\ 0 & V_I = V_o \end{cases}$$



What is VCO ?

- VCO is a circuit module that ***oscillates*** at a controlled frequency ω**.**
- The ***Oscillating Frequency*** is controlled using Voltage $V_{Control}$.
  - That is why the module is called
    - ***Voltage Control Oscillator***



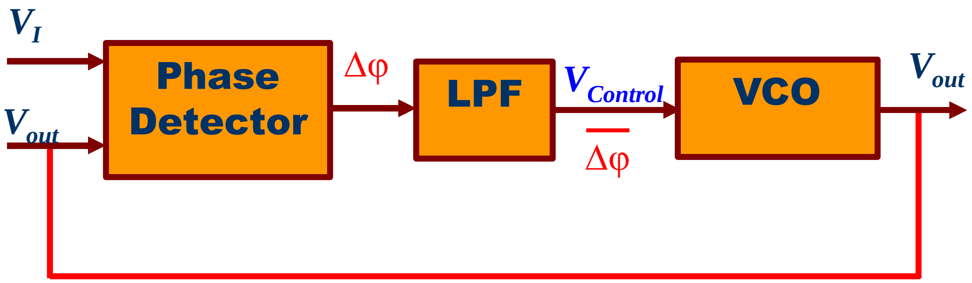


$$\omega = \omega_o + K_{VCO} V_{Control}$$

- $V_{control}$ must be in the steady state for the VCO to operate properly

Simple PLL

- Structure
  - Phase Detector (XOR) that detects the phase error Δφ
  - Low Pass Filter (to smooth Δφ)
  - Voltage Control Oscillator (VCO)
- Basic Idea
  - If V_I and Vout are out of phase (unlocked), then the PD module detects the error and the LPF smoothes the error signal. The control signal slows down or speeds up the VCO module; hence, the phase is corrected (locked)



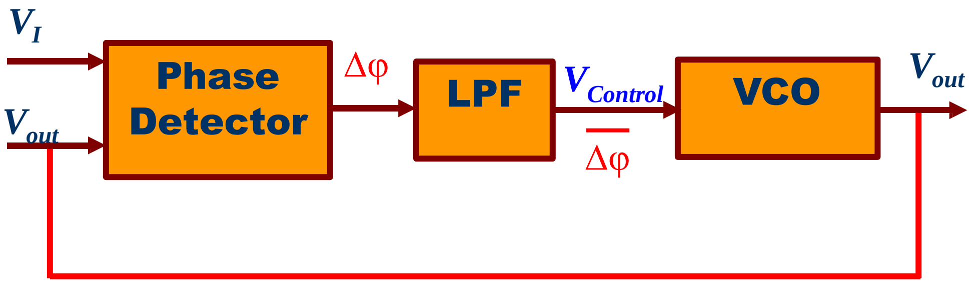
Locked Condition

- Locked Condition

$$\frac{d}{dt}\left(\varphi_{in}-\varphi_{out}\right)=0$$

- This implies that

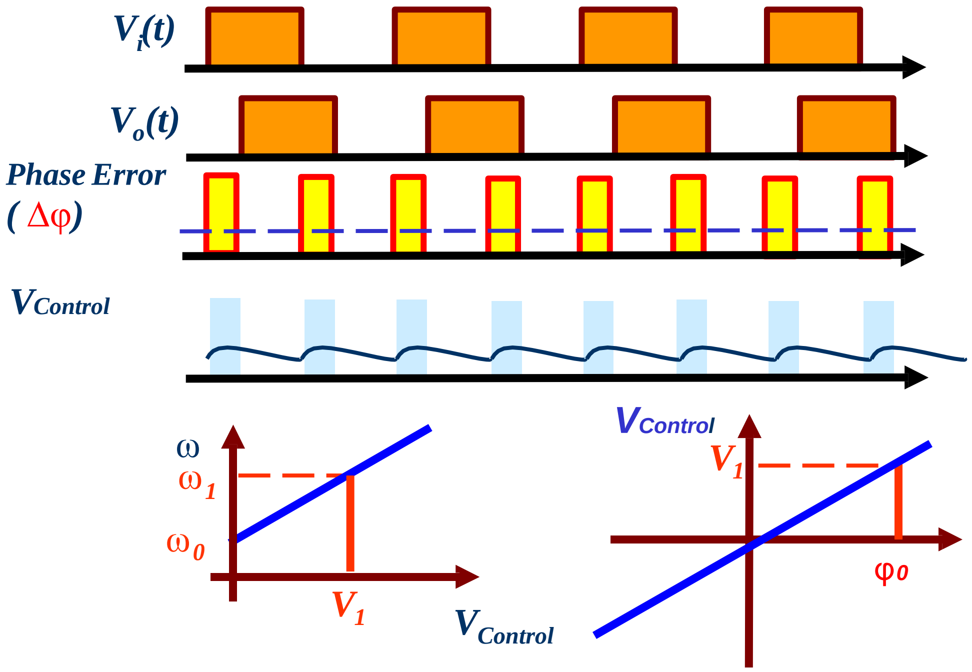
$$\omega_{in}=\omega_{out}$$



Example: In the UNLOCKED State

V_I and V_{out} has Δφ at the same frequency ω1

- The phase detector must produce V_I
- Hence, VCO is dynamically changing and PD is creating $V_{Control}$ to adjust for the phase difference.
- The PLL is in the Locked state



In the UNLOCKED State

- **For Simplicity** and by using **Fourier Series**
- Let $V_I = V_A \cos\left(\omega_1 t\right)$ $V_{out} = V_B \cos\left(\omega_1 t + \varphi_o\right)$
- Due to Δφ, PD creates V_{control}
- VCO will change

$$\omega_{out} = \omega_1 + K_{VCO} V_{Control}$$

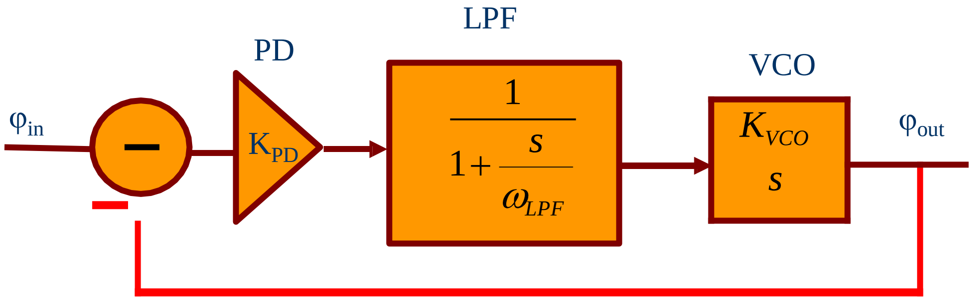
- The output voltage becomes

$$V_{out} = V_B \cos\left(\omega_1 t + \varphi_o - \Delta\varphi(t)\right)$$

Dynamics of Simple PLL

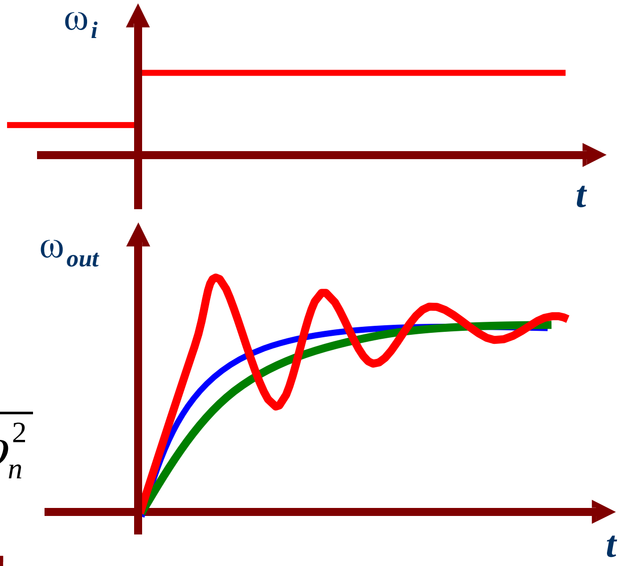
- PLL is a feedback system
  - PD is a gain amplifier
  - LPF be first order filter (as an example)
  - VCO is a unit step module
- The transfer function of the feedback system is given as:

$$H(s) = \frac{\Phi_{out}}{\Phi_{in}}(s) = \frac{\omega_{out}}{\omega_{in}}(s) = \frac{\omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2} \qquad H(s) = \frac{K_{PD}K_{VCO}\omega_{LPF}}{s^2 + \omega_{LPF}s + K_{PD}K_{VCO}\omega_{LPF}}$$

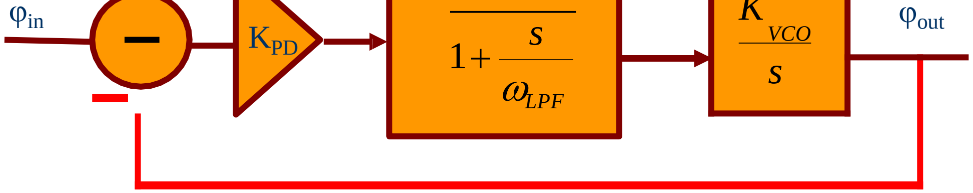


Transient Response to PLL

- The unit step response to second order system
  - Overdamped
  - Critically damped
  - Underdamped
- Problems with this PLL
  - Settling time Vs. ripple of Vcontor
  - Stability of the system
  - Lacks performance in ICs

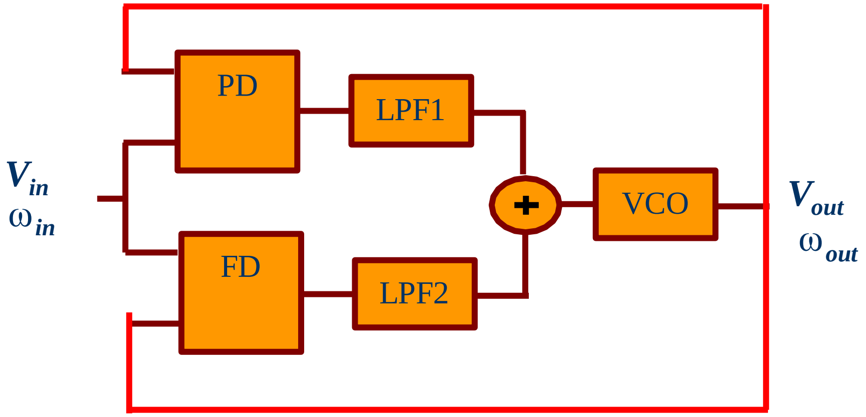


$$H(s)=\frac{\Phi_{out}}{\Phi_{in}}(s)=\frac{\omega_{out}}{\omega_{in}}(s)=\frac{\omega_n^2}{s^2+2\varsigma\omega_n s+\omega_n^2}$$



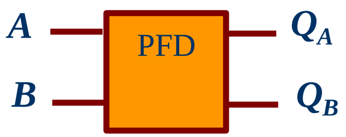
Problem of Lock Acquisition

- When PLL is turned on, the output frequency is far from the input frequency
- It is possible that the PLL would never lock
- Modern PLL uses FREQUENCY DEDECTOR (FD) in addition to the PD.



Phase/Frequency Detector (PFD)

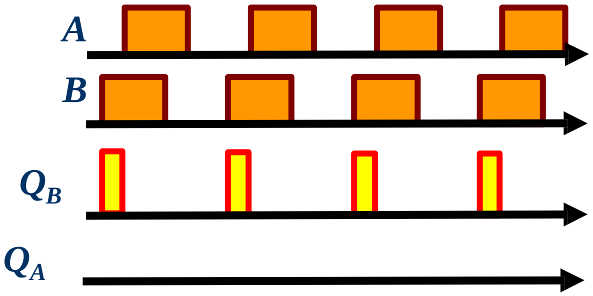
- One Module that detects both frequency and phase differences
- This module senses the transition in A or B

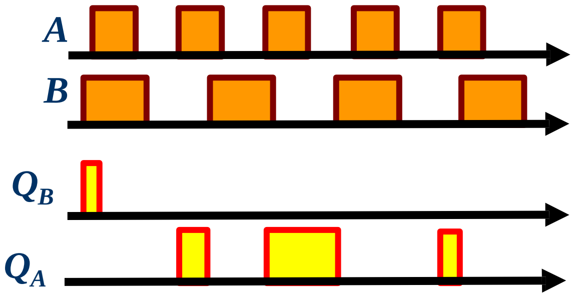


	A	B	QA	QB
Initially	0	0	0	0
A leads B	0 € 1	0 € 0	0 € 1	0 € 0
	XX	0 € 1	1 € 0	0 € 0

	A	B	QA	QB
Initially	0	0	0	0
B leads A	0 € 0	0 € 1	0 € 0	0 € 1
	0 € 1	XX	0 € 0	0 € 0

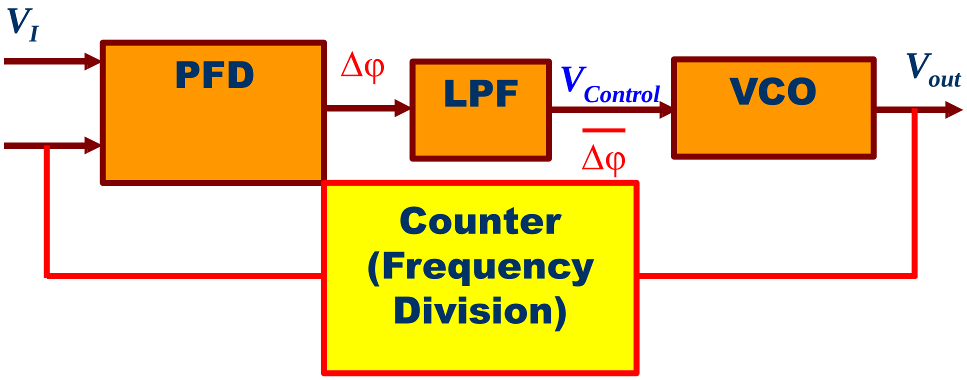
- If A leads B, Q_A changes its state and Q_B remains unchanged
- If B leads A, Q_B changes its state and Q_A remains unchanged





Application of PLL

- **Frequency Multiplications**
  - **The feedback loop has frequency division**
  - **Frequency division is implemented using a counter**



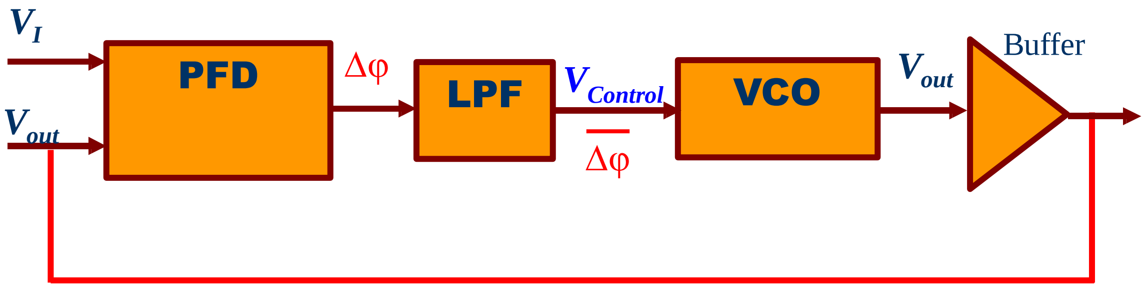
Clock Skew Reduction

Buffers are used to distribute the clock

Embed the buffer within the loop

Application of PLL

- Clock Skew Reduction
  - Buffers are used to distribute the clock
  - Embed the buffer within the loop



- Jitter Reduction